SPECIFICATION:

Please amend the paragraphs appearing at page 6, line 22 to page 7, line 15 as follows:

An irregular clock input [[110]] 105 arrives from a source clock and enters a finite state machine [[115]] 110, which functions as a frequency controller, allowing a single output signal for a specified number of input signals. The finite state machine [[115]] 110 is further connected to a rising or falling edge detector [[120]] 115 that outputs a one shot train signal to the monostable trigger [[125]] 120. The monostable trigger [[125]] 120 is variably comprised of inverse logic gates and delay latches. This output signal is the same frequency as the input signal, but significantly less than 50% duty cycle. Changes in voltage in a feedback loop, beginning at P100 (positive FET), further cleans the clock signal by forcing it to conform to an assumed ideal pulse shape. Inverters can perform the same function. The cleaned and conditioned signal is then passed independently to an inverter [[135]] 125, and to an operational amplifier (OPAMP) [[130]] 135.

The OPAMP [[130]] 135 is typically a high gain amplifier, with the negative input receiving a predetermined reference voltage from outside the monostable trigger [[125]] 120, and it is adjusted by the complementary signal difference between a reference voltage and the rising or falling edge detector voltage [[120]] 115. This in turn adjusts the force voltage at P100. A final integrating circuit [[140]] 130 blends the signal passed through the inverter [[135]] 125 and the reference signal arriving at OPAMP [[130]] 135 to obtain an average voltage equal to the design requirements of the system.